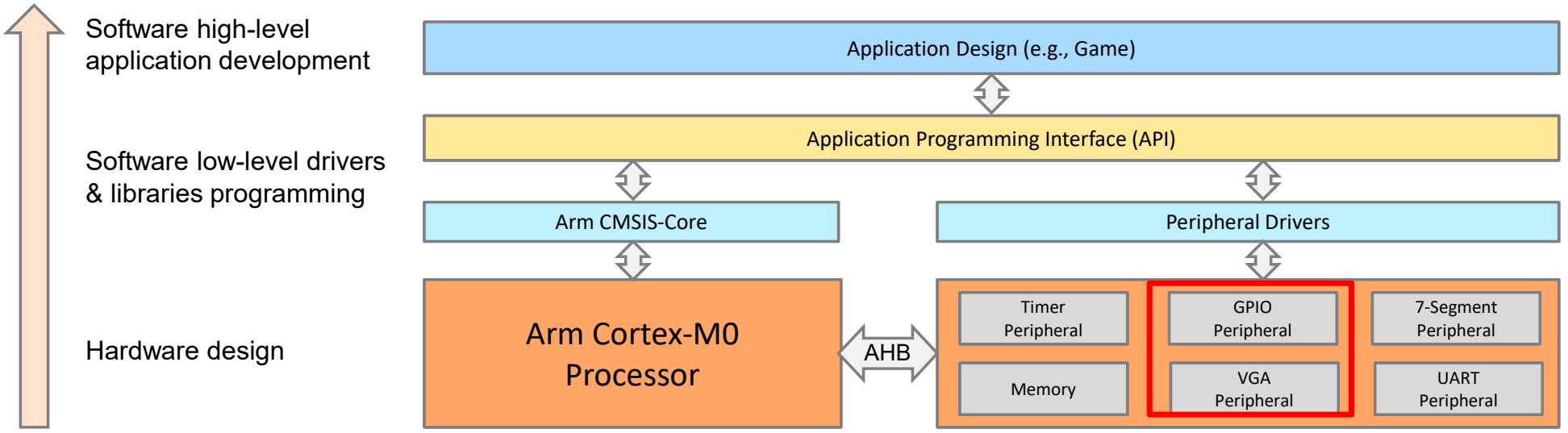
GPIO and VGA Peripherals

Agenda

Design and Implementation of

- AHB GPIO Peripheral
- AHB VGA Peripheral

Building a System on a Chip (SoC)



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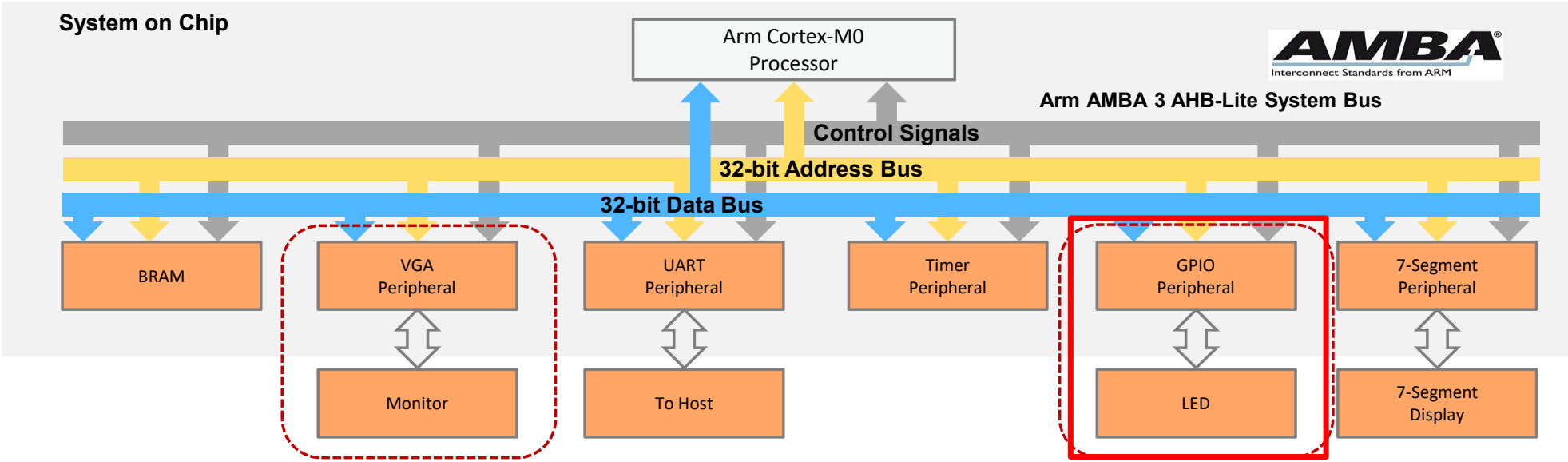
Hardware Module Overview



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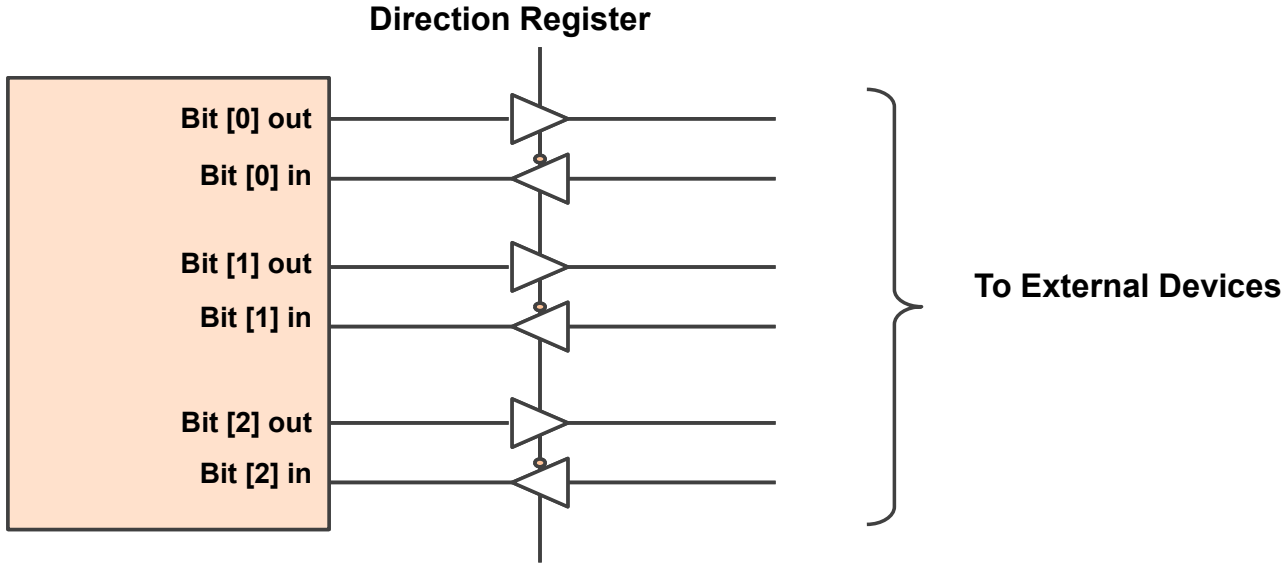
GPIO Overview

General-purpose input/output (GPIO)

- Used for general purpose; no special usage defined
- Widely used in most applications
- The direction of input/output is controlled by the direction register.
- A mask register is often used to mask out certain bits.



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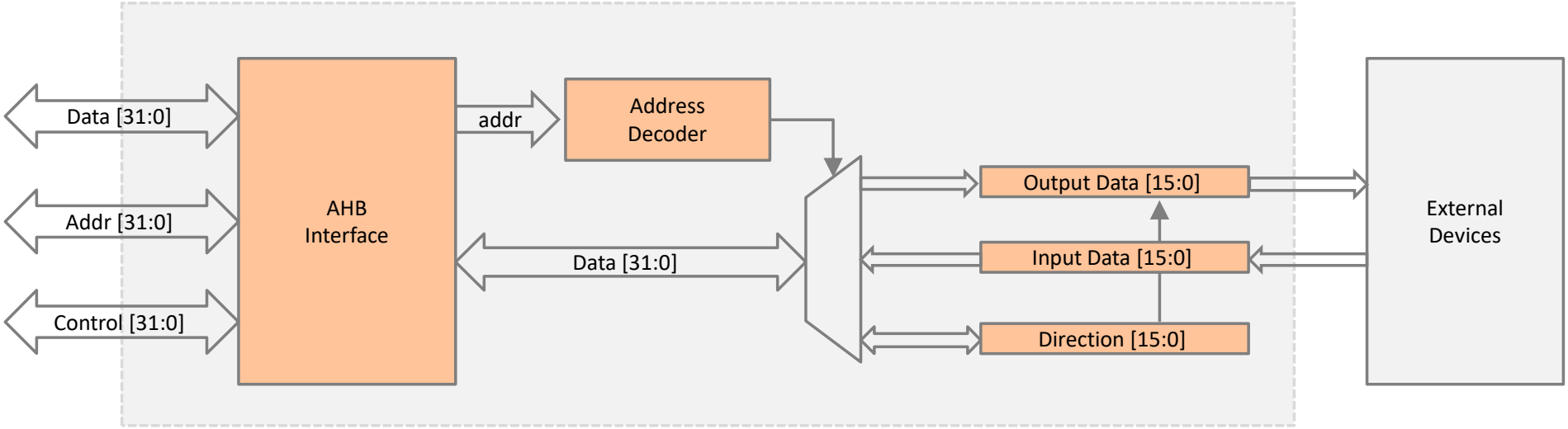
AHB GPIO

Basic hardware architecture

- Only has the basic registers, namely data in, data out, and direction register
- Note that only Direction[0] is used in the example RTL
- Does not have a mask register or any other functions



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GPIO Registers

The GPIO peripheral registers include

- Data registers
  - Input data: the data read from external devices
  - Output data: the data sent to external devices
- Direction register
  - Controls whether it is a read or write operation

Register	Address	Size
GPIO base address	0x5300_0000	
Data	0x5300_0000	16 bits
Direction	0x5300_0004	16 bits

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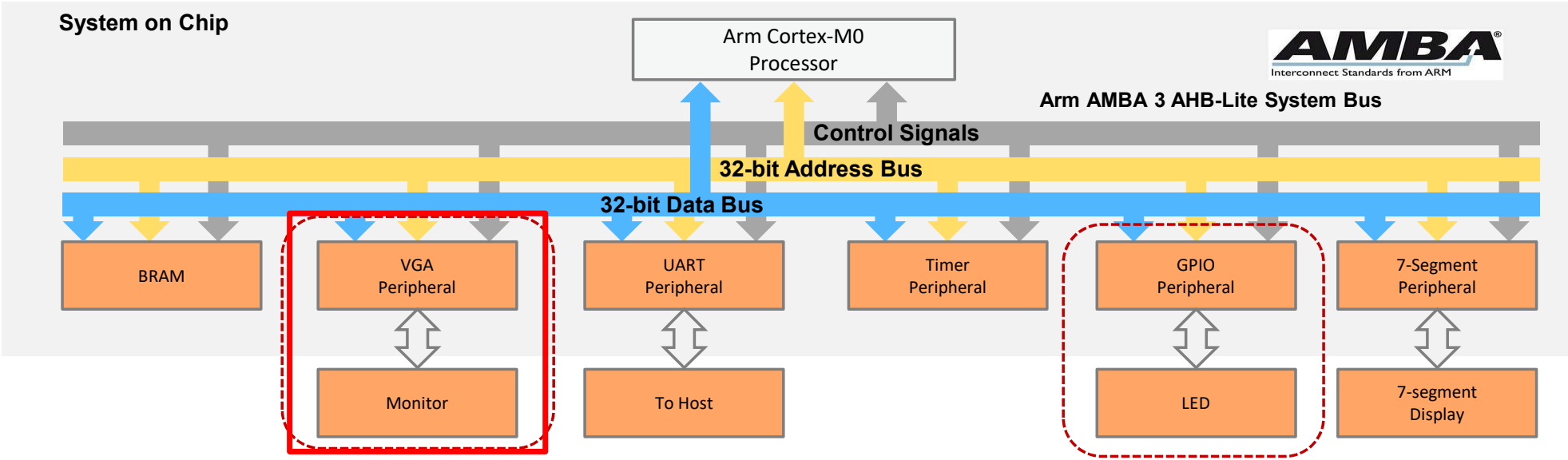
Hardware Module Overview



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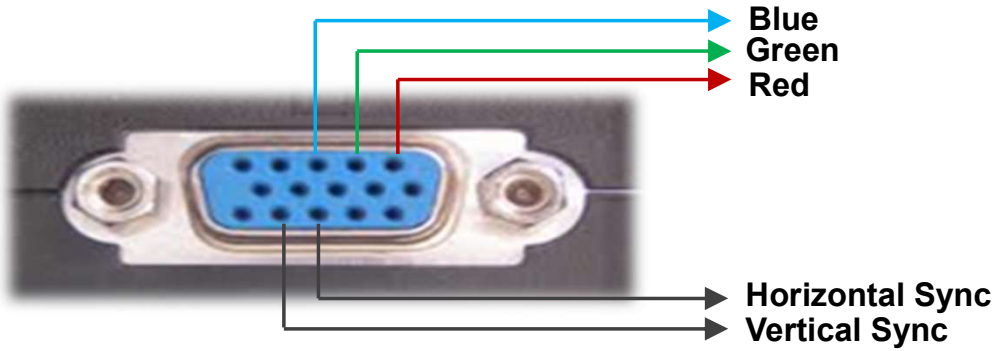
VGA Overview

VGA connector

- Five analog components
- Blue, green, red
- Horizontal and vertical synchronization
- Designed in 1987 and still used nowadays, most of them are superseded by digital visual interface (DVI) and high-definition multimedia interface (HDMI).



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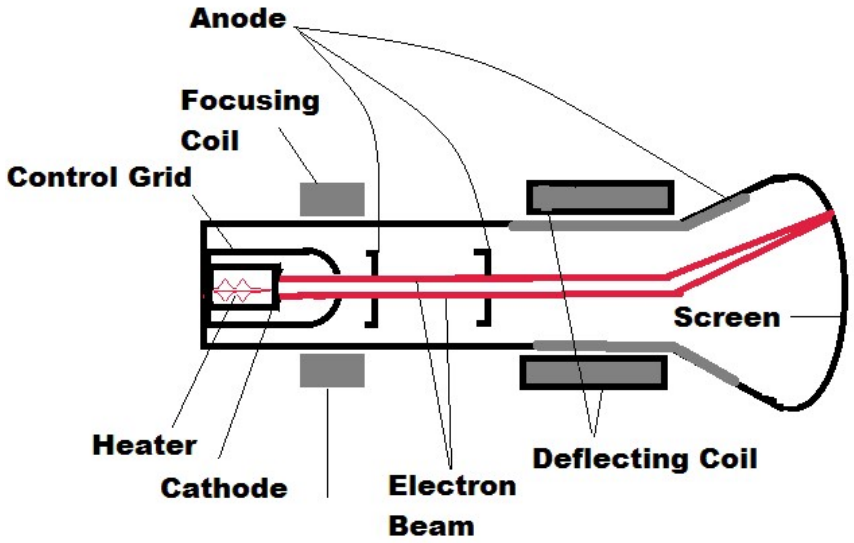
How VGA Signals Work

CRT monitors display images on a phosphor-coated screen using amplitude-modulated moving electron beams as shown in the figure below.

Beams horizontally move from left to right, and vertically from top to bottom.

As the beam moves over the whole screen, the colour information of the pixel that is currently being scanned is given from the VGA cable.



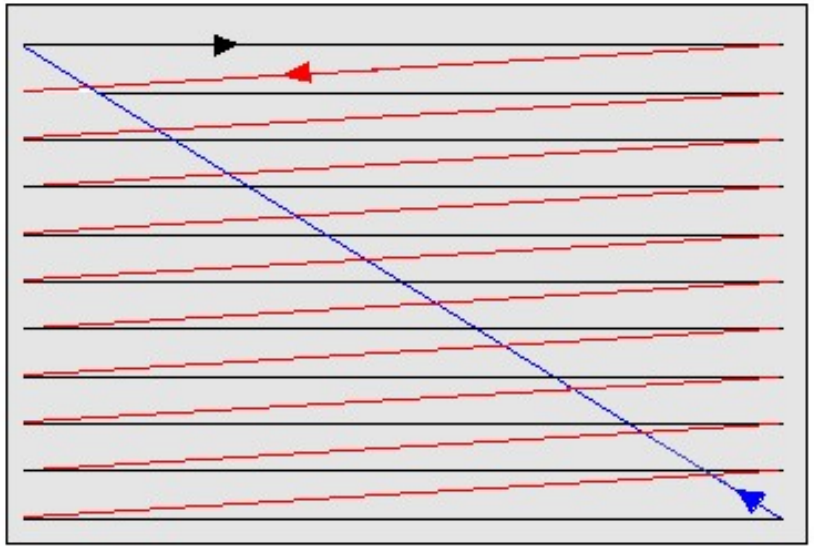
Cathode Ray Tube

How VGA Signals Work

The horizontal synchronization is used to reset the beam to the start of the next line.

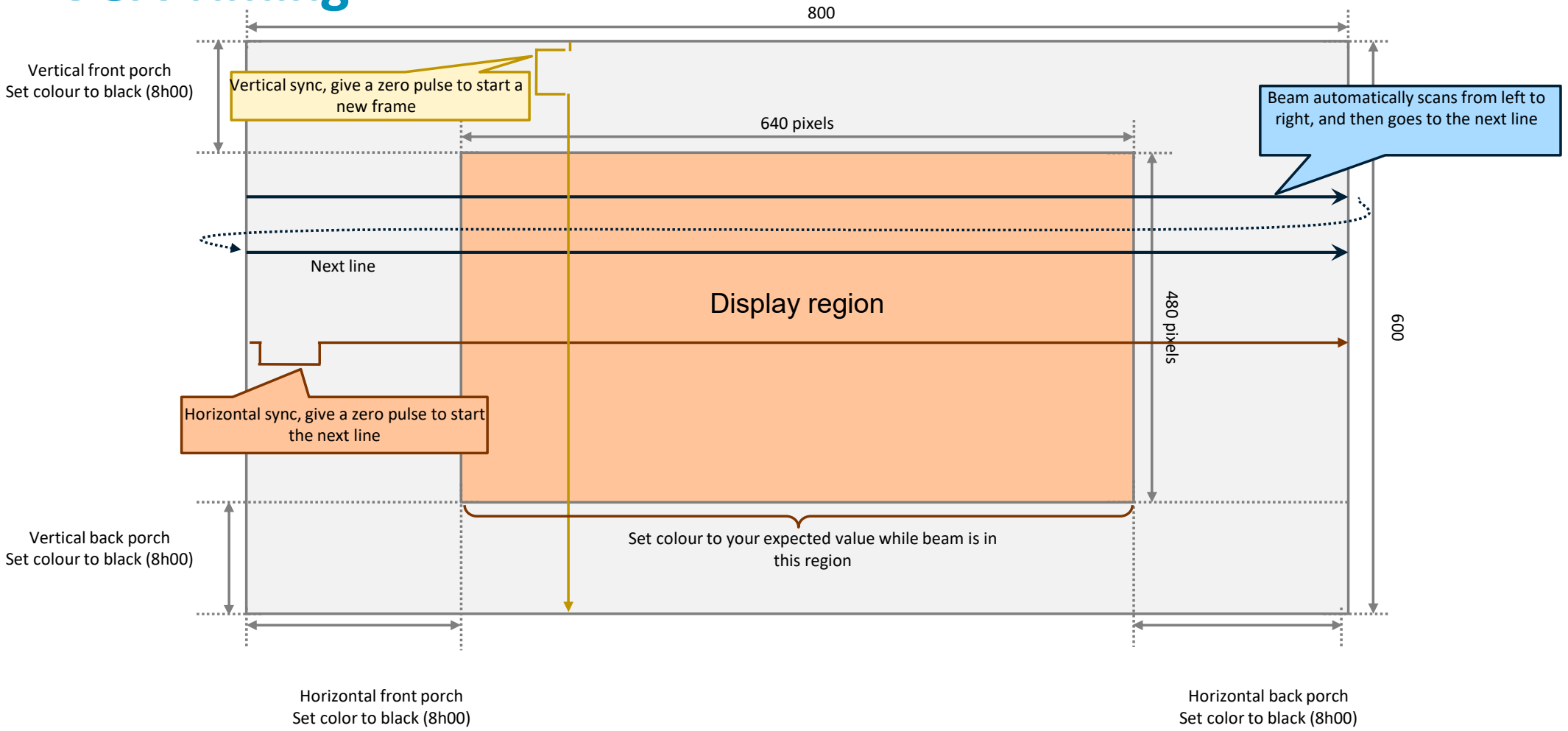
The vertical synchronization is used to start the next frame.

The monitor will adjust its scanning frequency and screen resolution according to the synchronization signal given from the user.



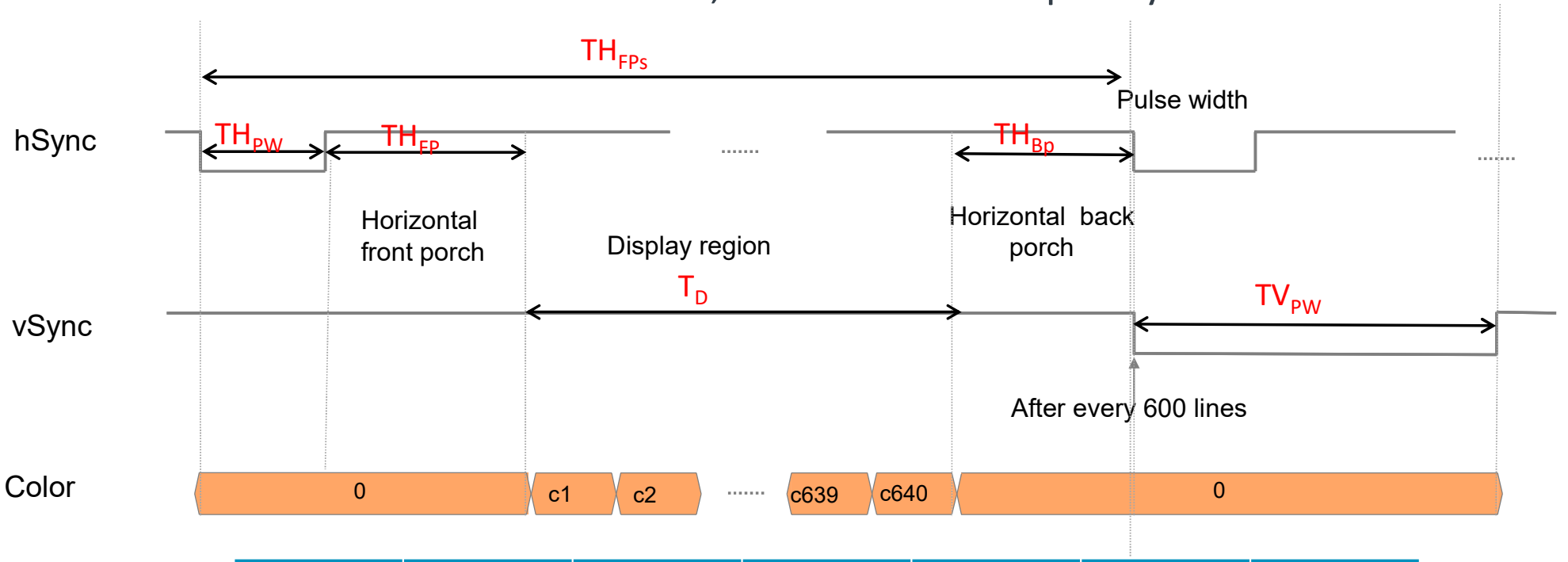
Raster Scanning

VGA Timing



VGA Timing

For monitor with 640 × 480 resolution, 25 MHz clock frequency and 60 Hz refresh rate:



Symbol	TH_{PW}	TH_{FP}	TH_{BP}	Ts	T_D	TV_{PW}
Time(s)	3.84u	640n	1.92u	16.7m	15.36m	64u

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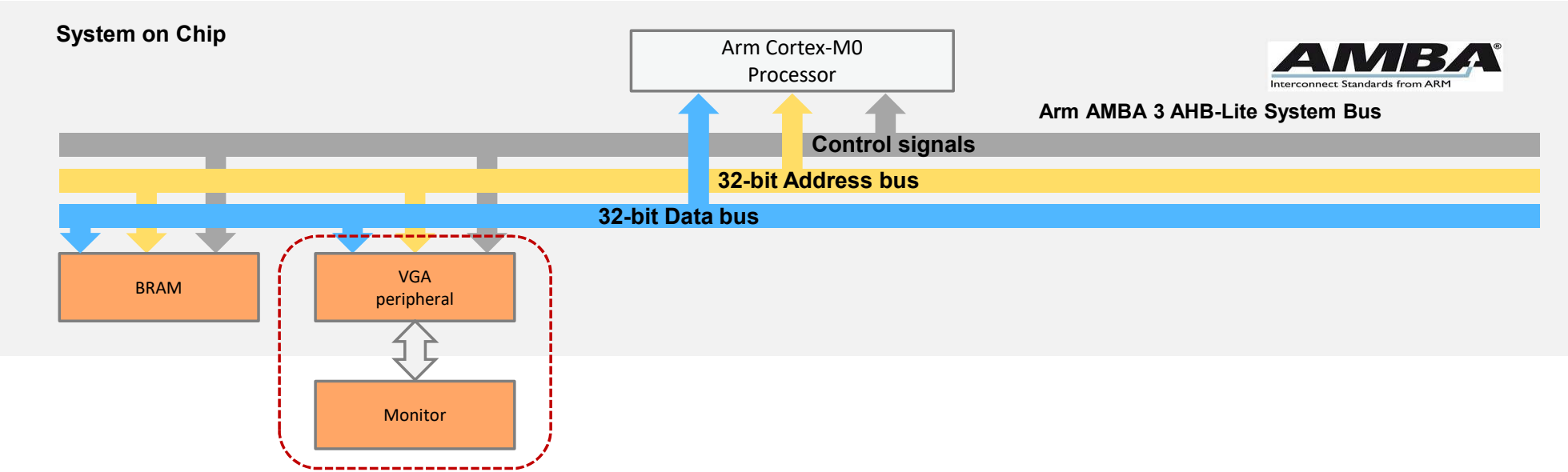
AHB VGA Peripheral



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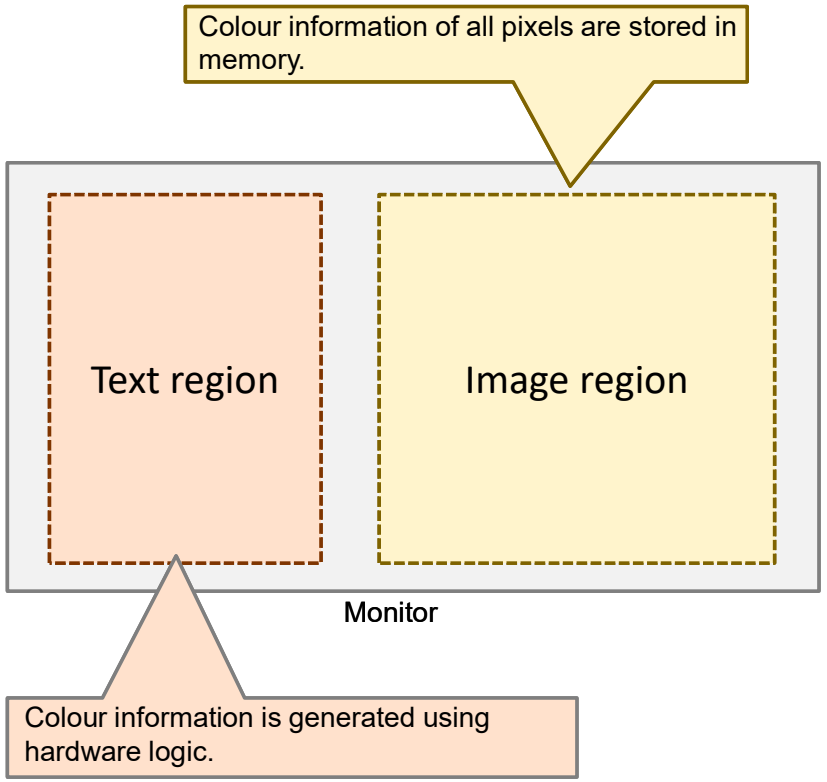
Additional Design Requirement

The full region of the screen is divided into two subregions:

- Text region (console): first 240 pixels horizontally : displays text strings in a relatively high resolution
- Image region (frame buffer): displays a desired image in a lower resolution

Separate storage locations for image and text are needed to compensate for insufficient space in the on-chip memory.



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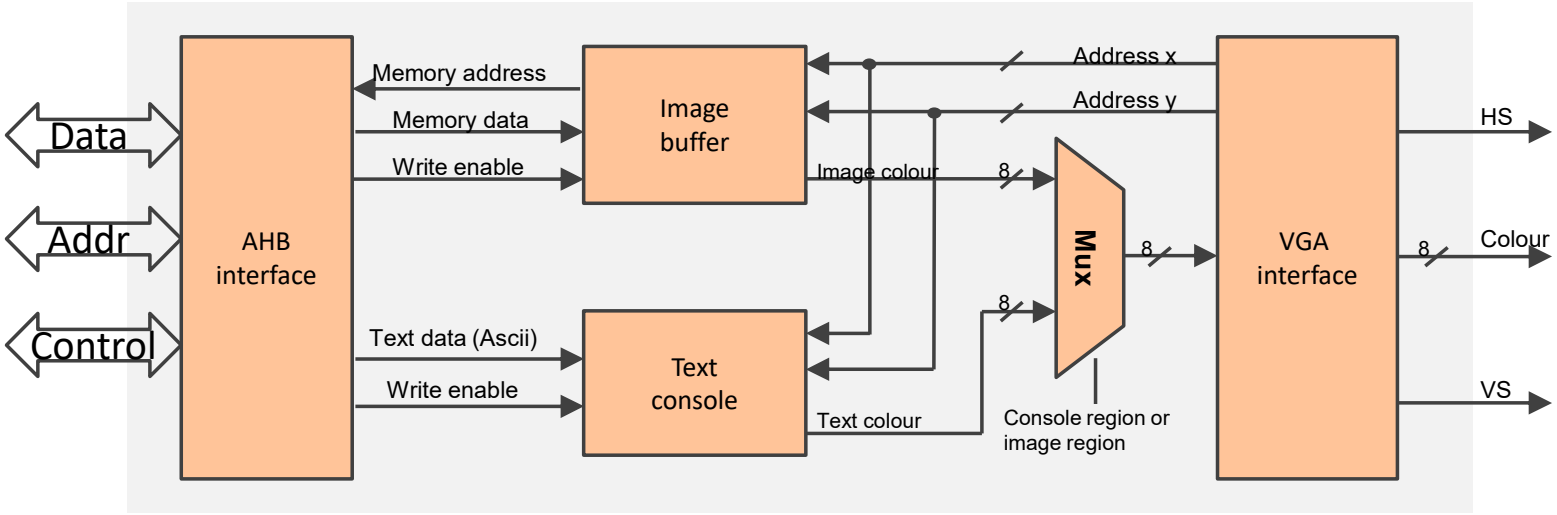
AHB VGA Peripheral Hardware Architecture

The VGA peripheral can display texts and images on a monitor through a VGA cable.

The VGA peripheral consists of 5 components: , an AHB interface, a VGA interface, an image buffer for displaying images, a text console module for displaying texts, and a multiplexer.



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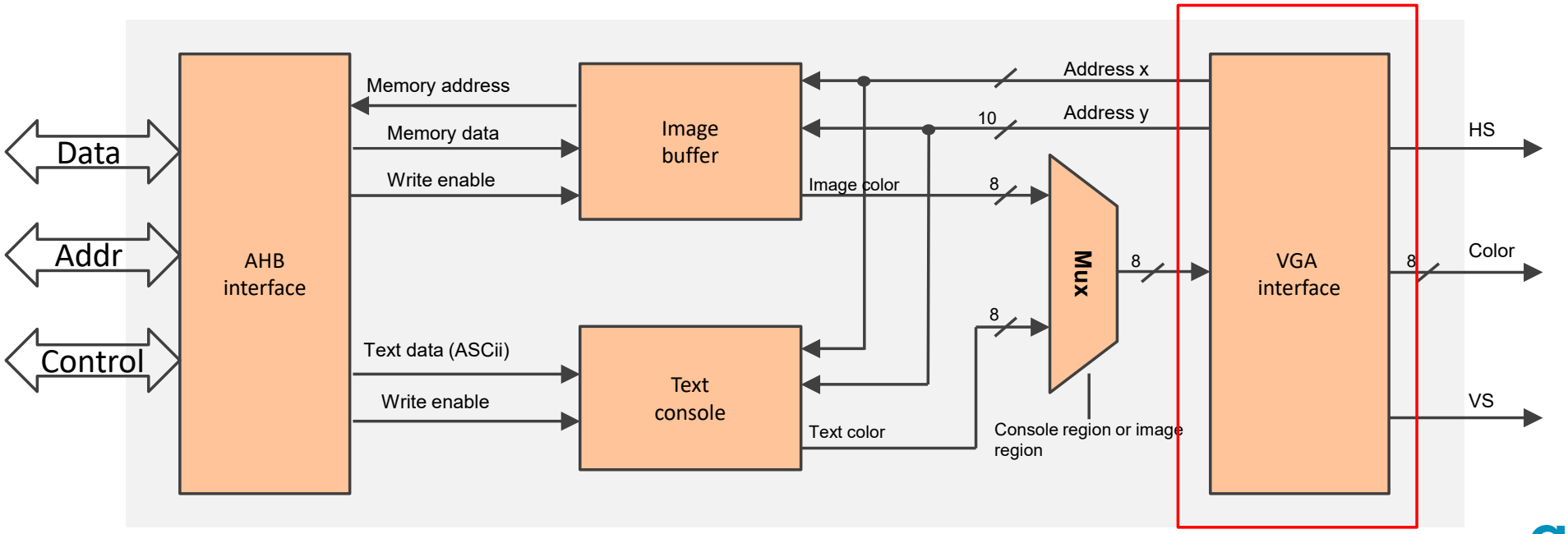
VGA Interface

- Generates synchronization signals to the VGA port
- Is directly connected to external pins of the VGA port
- Outputs the address of the current pixel



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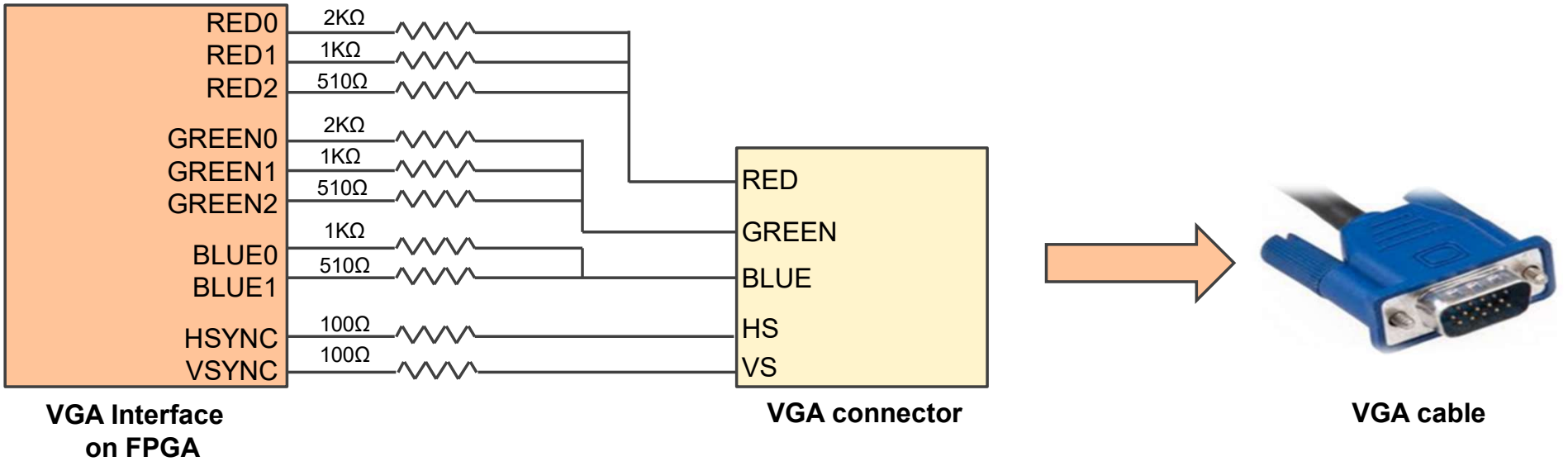
VGA Interface

- The digital outputs from the FPGA can be converted to analogue and connected to the VGA connector using resistor-divider circuits.
- The example below utilizes 10 signals, including 8-bit color and two standard sync signals; thus, 256 color levels can be presented.



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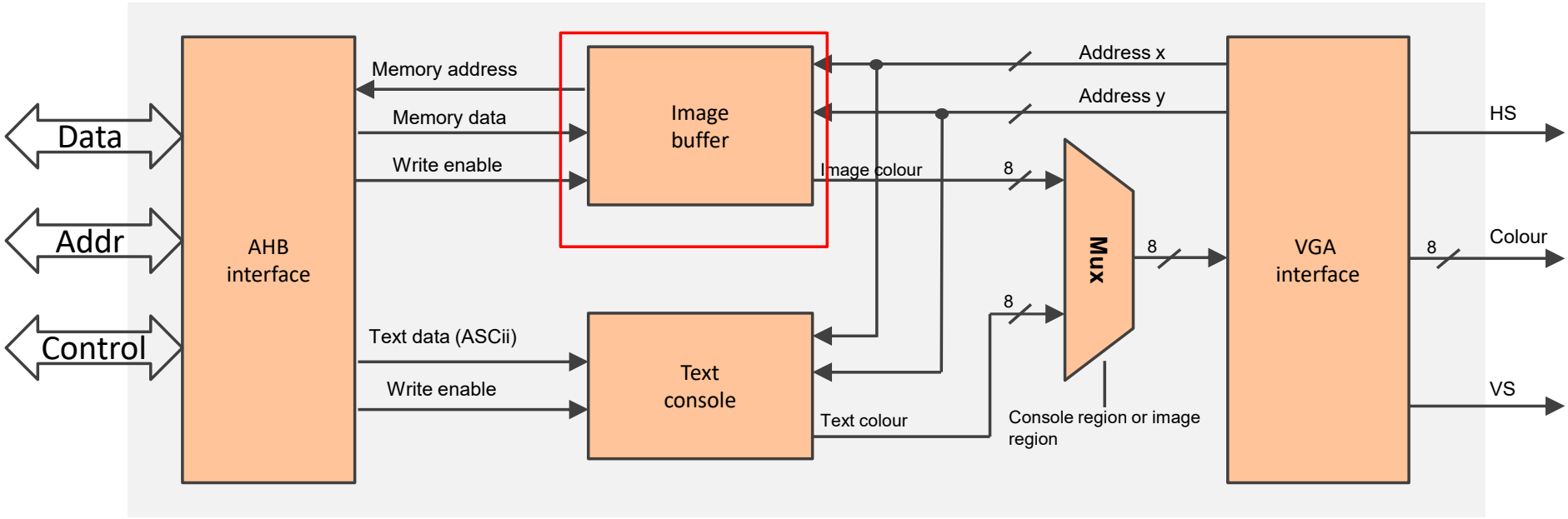
VGA Interface

VGA signals

Name	Description
vga_red[2:0]	3-bit red signal
vga_green[2:0]	3-bit green signal
vga_blue[1:0]	2-bit blue signal (less sensitive to eyes)
hsync	Horizontal synchronization signal: one pulse indicates the start of the next line.
vsync	Vertical synchronization signal: one pulse indicates the start of the next frame.

VGA Image Buffer

- Stores the colour information of all pixels in the image region
- Is implemented as a dual-port memory



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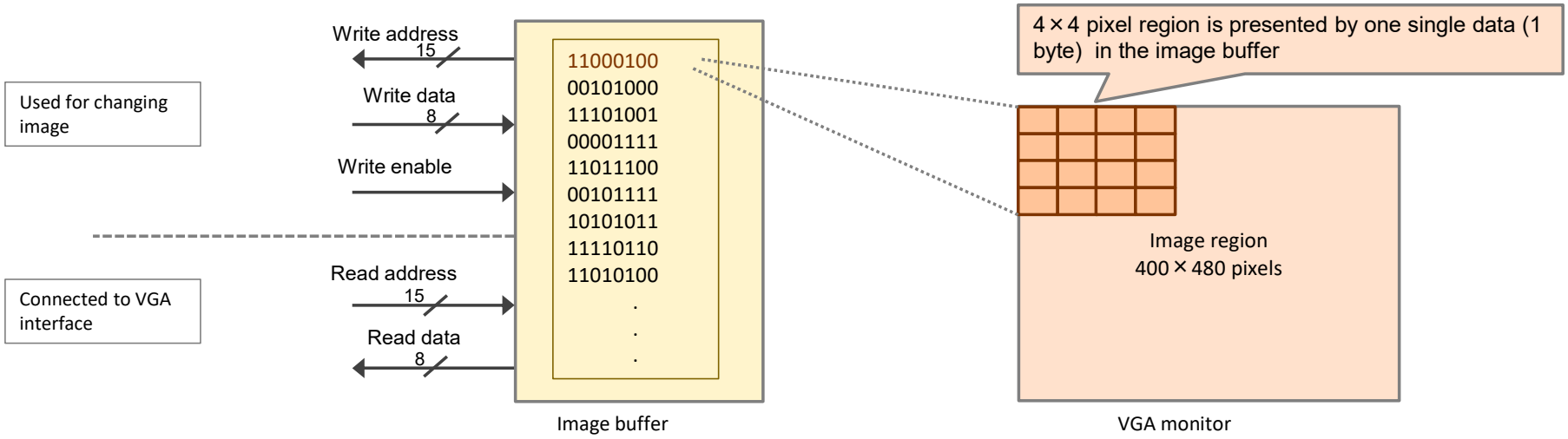
VGA Image Buffer

Some chips do not have a large on-chip memory, such as on-chip SRAM. In such a case, the resolution can be reduced by mapping multiple pixels to a single data in the memory. For example, a 4 × 4 pixel region can be presented by one single data entry in the image buffer.



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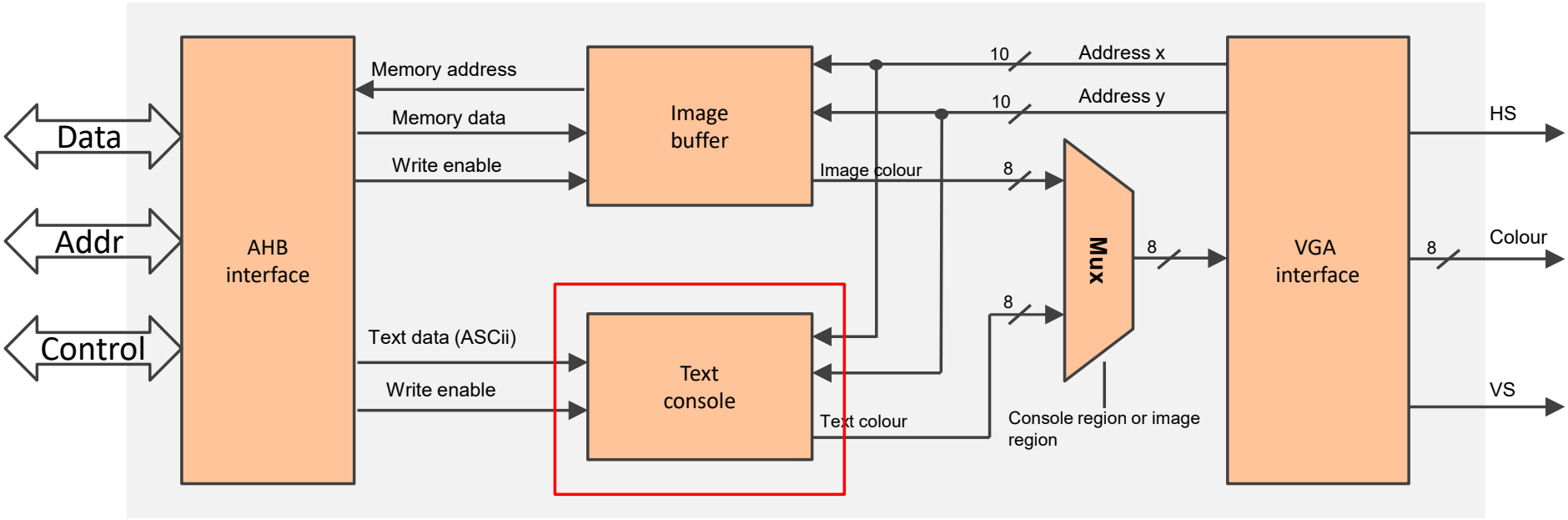
Text Console

- Displays texts in the text region
- Is implemented as hardware logic



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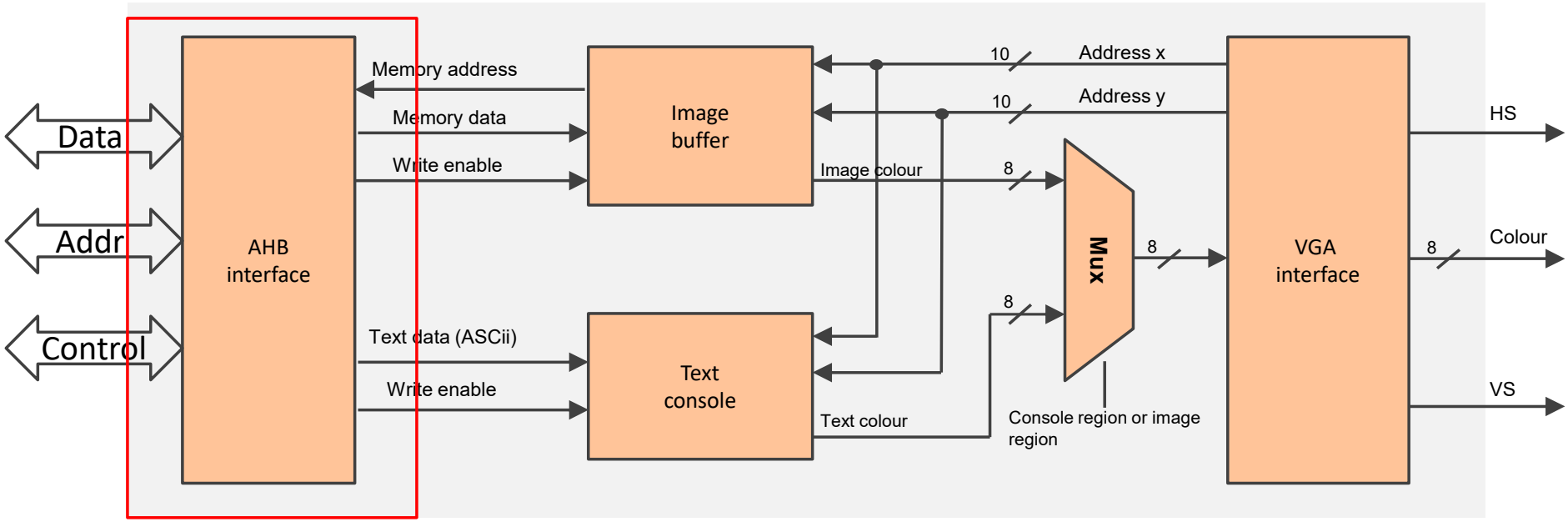
AHB Interface

- Manages the flow of data and control signals between the AHB bus and the VGA peripheral internal memories



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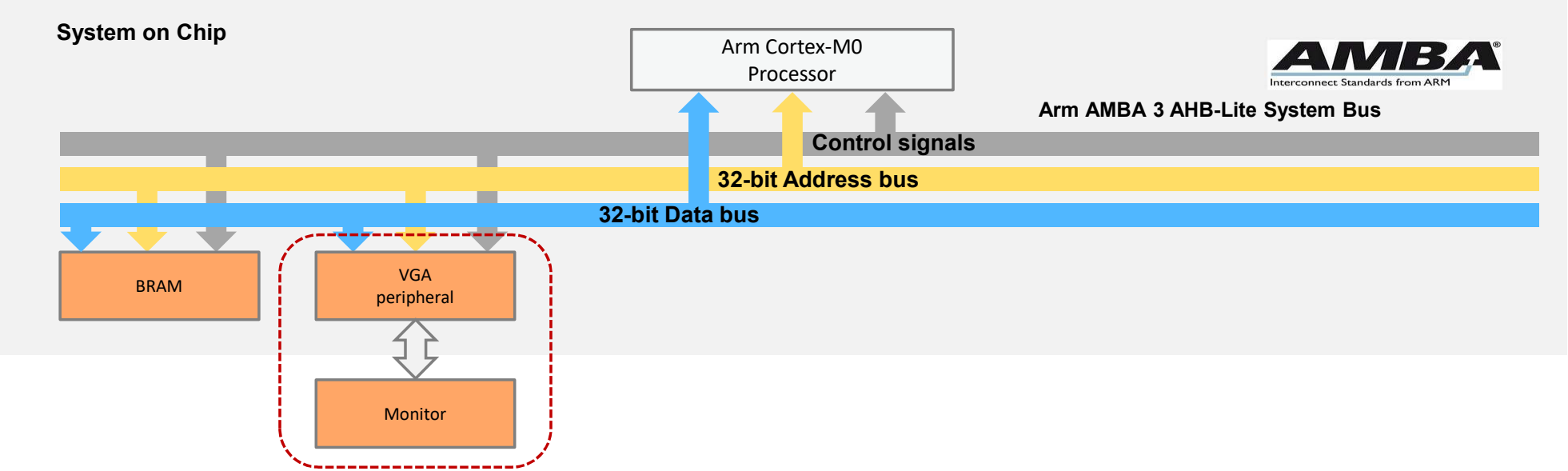
Memory Space

The memory space is allocated as follows:

Peripheral	Base address	End address	Size
MEM	0x0000_0000	0x0FFF_FFFF	16MB
VGA	0x5000_0000	0x50FF_FFFF	16MB



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Memory Space

The internal memory space of VGA is divided into two regions:

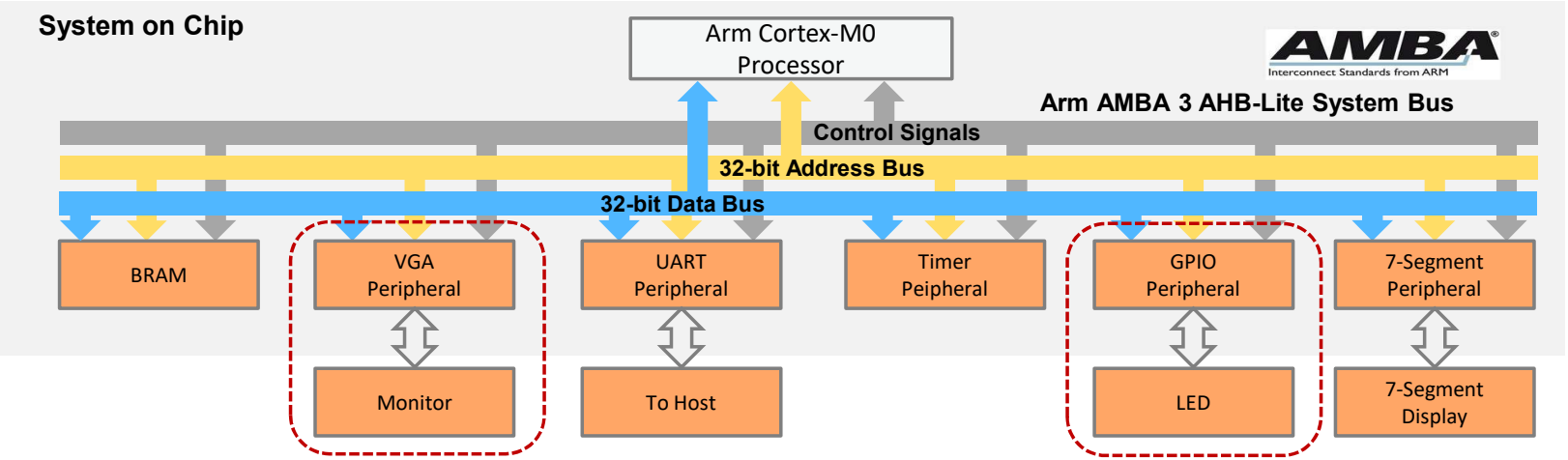
- Console text: 1 word (4 byte) to print a character
- Image buffer: the rest of the memory space is used to store pixels in the image region.

Register	Base address	End address	Size
Console text	0x5000_0000	0x5000_0000	4 Byte
Image buffer	0x5000_0004	0x50FF_FFFF	(16M-4) Byte

Memory Space

The memory space for all peripherals is allocated as follow:

Peripheral	Base address	End address	Size
MEM (BRAM)	0x0000_0000	0x4FFF_FFFF	167MB
VGA	0x5000_0000	0x50FF_FFFF	16MB
UART (not included)	0x5100_0000	0x51FF_FFFF	16MB
Timer (not included)	0x5200_0000	0x52FF_FFFF	16MB
GPIO	0x5300_0000	0x53FF_FFFF	16MB
7-segment (not included)	0x5400_0000	0x54FF_FFFF	16MB



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