Aadi Desai

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Education

Imperial College London *Oct 2019 – Jun 2023*

Master of Engineering in Electronics and Computer Engineering | **First Class with Honours**

Skills

Rust, Go, Git, Cloudflare Workers, TypeScript, Python, C++, PostgreSQL, Docker Compose, Solidity, F#, SystemVerilog

Projects

IRC-style Chat Server and Terminal Client GitHub: supleed2/go-chat *Dec 2023 – Jan 2024*

- Built a chat server and client, providing a terminal user interface using the Elm architecture
- Types are imported to client and server code, maintaining a single source-of-truth for communication
- Clients connect to the server using WebSockets, and exchange messages via JSON
- Server maintains recent chat history for multiple rooms, rooms can be created / destroyed on-demand
- Go learning project, including WebSockets, Goroutines and Channels for message passing
- Used mutexes to avoid race-conditions and concurrency bugs when shared data can be written to

Automated Verification Discord Bot GitHub: supleed2/nanobot *Jul 2023 – Aug 2023*

- Developed a Discord bot for member onboarding, built on the Poise framework and the Shuttle platform
- Replaces manual checks for Imperial student status, as requests were often missed during busy periods
- Running since August 2023 with minimal downtime, allowing members to join quickly and independently
- Leverages Cloudflare Pages + Functions to query the university API without storing sensitive login credentials
- Rust learning project in a real-world environment, with active users providing feedback

Final Year Project: FPGA Accelerator for StackSynth GitHub: supleed2/EIE4-FYP *Oct 2022 – Jun 2023*

- Created a LiteX + SystemVerilog project to generate audio on a custom OrangeCrab FPGA accelerator board
- Intended for use in the 3rd Year Embedded Systems module of the Imperial Electrical Engineering course
- LiteX wrapper module connecting the custom designs and existing IP, e.g. the integrated RISC-V CPU, VexRiscV
- Designed SystemVerilog modules which are instantiated in the LiteX wrapper: a CAN-bus receiver to accept messages from connected StackSynth boards, a 64-channel 48kHz configurable wave sample generator
- Includes C++ demo software for the integrated CPU, to be replaced with student-written coursework code

Experience

Graduate Software Engineer – Ultra Intelligence & Communications *Sep 2024 – Present*

- Built out strategic proof-of-concept prototypes to stress-test and demonstrate early-stage projects, transforming ideas into working products to validate potential product opportunities

Junior Embedded Software Engineer – Prolec Ltd *Apr 2024 – Aug 2024*

- Working on automated safety systems for construction and excavation equipment, including the ability to restrict power and prevent equipment from entering dangerous areas or unstable positions
- Overhauled the C++ codebase to reduce code size, via conditional compilation and reduced class inheritance, providing space for new features on existing space-constrained hardware
- Implemented the J1939 messaging protocol atop the CAN bus, including handshakes to confirm safety-critical requests, allowing the product to run headless with an external display

Digital Design Engineer – Nordic Semiconductor *Apr 2022 – Sep 2022*

- Developed open-source tooling for syntax highlighting and configurable style / syntax linting of SystemVerilog
- Updated SystemVerilog simulation designs to use only synthesizable constructs, for Verilator compatibility
- Gathered feedback from colleagues for improvements to the editor tooling, such as linting rules to add