Aadi Desai

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Profile

1st Class MEng graduate of Electronics and Information Engineering at Imperial College London, looking to start their career in Software and Hardware Engineering. Experience with embedded and systems programming and architecture design, most recently in Rust**.** Interested in learning high-performance and low-level computing.

Education

Imperial College London *Oct 2019 – Jun 2023*

Master of Engineering - MEng, Electronic and Information Engineering

Award: **1st - First Class with Honours** *transcript available on request*

Favourite Modules:

Advanced Computer Architecture • Coding Theory • Control Systems • Cryptography Engineering • Digital and Computer Architecture • Digital Systems Design • Discrete Maths • Embedded Systems • Hardware and Software Verification • High Level Programming • Information Processing • Instruction Architectures and Compilers • Music Technology • Network and Web Security • Principles of Distributed Ledgers • Program Analysis • Software Reliability • Software Systems • Type Systems for Programming Languages

Queen Elizabeth's School, Barnet *Sep 2017 – Aug 2019*

A-Level Subjects: Mathematics (A*), Further Mathematics (A), Physics (A*)

AS-Level Subjects: Mathematics (A), Further Mathematics (A), Physics (A), Design & Technology: Product Design (A)

Skills

Used in Academics: C • C++ • F# (Basic Familiarity) • Intel Quartus Prime • LiteX • SystemVerilog

Used in Personal Projects: Rust • Python • Docker + Compose • Cloudflare DNS + Pages + Workers

Experience & Accomplishments

Digital Design Engineer – Nordic Semiconductor *Apr 2022 – Sep 2022*

Goal: research open-source tooling to improve the testing and development workflow of RTL in SystemVerilog within the company, focusing on Verilator for its speed in simulation and robust linting options. Outcomes include:

- SystemVerilog syntax highlighting using a VSCode extension and user or company configurable syntax and style linting rules on files opened by the editor. Communication with team members was vital as decisions about linting rules and functionality of the VSCode extension were informed by direct feedback.
- Updated SystemVerilog files, replacing simulation-specific constructs with synthesizable equivalents for Verilator compatibility and improved readability.

VEX EDR International Robotics Competition *Sep 2017 – May 2018*

Won awards in regional competitions and progressed to the UK national event, securing a finalist place, and qualifying our team for the International Event held in Kentucky, USA, where we represented the UK.

Goals: Design, build and test structural components of the VEX EDR robotics system, including compensating for known unreliable DC motors and encoders using Proportional–Integral–Derivative controllers on the central computer. Program the robot to compete in the assigned game and adjust for expected unknowns such as opponent position and target location. Testing and debugging of the various modules that made up the robot.

Store Volunteer – St Luke’s Hospice *Nov 2014 – Apr 2018*

Gained experience managing a store working on the sales floor and in the storage room, initially as part of the Duke of Edinburgh Award. Continued volunteering for multiple years as the experience working with new team members and customers was rewarding. Trained new volunteers as they joined and took on leadership roles as necessary.

Projects

Automated Verification Discord Bot GitHub: supleed2/nanobot *Jul 2023 – Aug 2023*

Access to a University Society Discord server is limited to Imperial students, and previously this access was manually maintained by the society committee, sometimes causing missed requests. This project involved creating a Discord bot to automatically handle verification of student status and make manual reviews more streamlined, motivated by my desire to learn the Rust programming language through building. The main components of the project are:

- Discord bot: using the Rust Poise (Discord API) framework, built to run on the Shuttle platform.
- Website: using Cloudflare Pages and Functions to check login credentials against the University API without storing sensitive login credentials, and passing the result of the check to the Discord bot.

Final Year Project: FPGA Accelerator for StackSynth GitHub: supleed2/EIE4-FYP *Oct 2022 – Jun 2023*

StackSynth is an educational synthesiser platform for real-time programming, used in the 3rd Year Embedded Systems module of the Electrical Engineering course at Imperial College London. This project greatly increased the audio capabilities and performance of the platform using a custom OrangeCrab FPGA accelerator board. During the project, the following designs were developed in LiteX (Python-based Domain Specific Language) and SystemVerilog:

- LiteX wrapper: to contain and connect the individual SystemVerilog modules and provided IP cores.
- CAN receiver: to communicate (receive only) with the existing StackSynth platform correctly.
- 48kHz sample generator: 64 individual oscillators, each with waveform shape and frequency control.
- C++ demo software for the integrated RISC-V CPU (VexRiscV) to be replaced by student software.

Home Lab / Server *Jul 2021 – Aug 2021*

Installed a local server as a space for other projects to be deployed to and a sandbox to experiment with different tools or languages. Initially driven by the goal to automate more devices within the house, avoiding the need to buy expensive hardware that could result in vendor lock-in or incompatibilities.

- Raspberry Pi 4B running Debian and Home Assistant, with access via Cloudflare Tunnels which handles TLS certificates, and avoids issues with port-forwarding due to being behind a CG-NAT after switching ISPs.
- Recompiled the RPi4B 64-bit kernel with the AppArmor Linux Security Module enabled to meet Home Assistant server hardening recommendations and achieve “Officially Supported” status.
- Upgraded bedside, bedroom and office lights to smart lights using ESP32/Shelly hardware running ESPHome.
- Expanded to support extra applications, e.g., uptime monitors and self-hosted apps, also exposed using Cloudflare Tunnels via subdomains, and access to the local network using Cloudflare Zero Trust.

EE2Rover Group Project *Apr 2021 – Jun 2021*

Goal: Design and build a rover with the ability to operate in a remote location autonomously, including reacting to and navigating through obstacles identified using an onboard camera. Design a remote-control interface with asynchronous instruction delivery so the rover could continue in the case of temporary loss of communication.

- Programmed the central ESP32, hosting the control interface and communication channels to the other modules. Developed teamwork while each member had authority over different areas of the project.
- Identified communication standards for transfer of status information and commands between Rover modules, using 2-wire UART and the ArduinoJSON library for consistent implementation in all modules.

MIPS-Compatible CPU Group Project *Oct 2020 – Dec 2020*

- Designed a synthesizable MIPS-compatible CPU using a memory-mapped interface for peripherals.
- Developed a custom Avalon-compatible communication module to convert the original bus design.
- Migrated the interface design, which used separate bus interfaces for instruction and data memories, to the more complex Intel Avalon standard. This enabled evaluation of the CPU design alongside other standard Avalon-compatible modules.